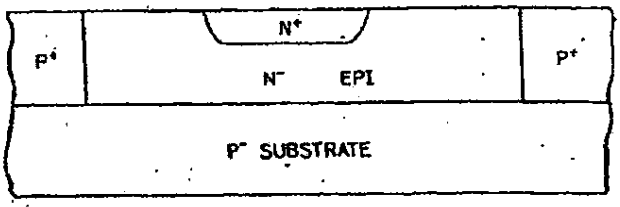
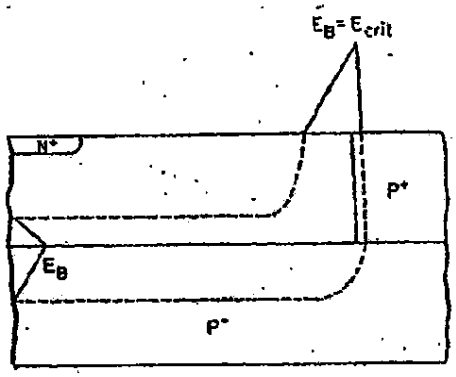


Fig. 5.1. CROSS SECTION OF A RESURF DIODE.

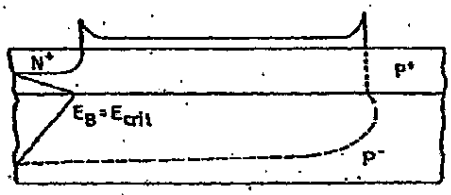
surrounded by P^+ isolation diffusion. When the diode is reverse biased, avalanche breakdown can occur at the vertical P^+N^- junction (surface breakdown) or at the horizontal P^-N^- junction (bulk breakdown). It has been observed [5.5,5.6] that the diode with a thinner N^- layer exhibited a considerably higher breakdown voltage than did the one with a thicker layer.

To achieve a better understanding of this behavior, a diode with a very thick epitaxial layer is first considered. Based on the one-dimensional plane-junction approximation, the vertical P^+N^- junction is one-sided, which is in contrast to the two-sided horizontal P^-N^- junction and, as a result, the critical field will first be reached at the surface. With thick epitaxial layers, the depletion at the surface of the vertical P^+N^- is not influenced by the horizontal junction because the horizontal P^-N^- is considered to be disconnected from the N^+ contact. Breakdown voltage is determined, therefore, by the P^+N^- junction whose electric-field pattern is shown in Fig. 5.2a.

As the epitaxial layer is made thinner, the depletion region will move from the bottomside horizontal junction toward the surface. If the layer is made thin enough so that the depletion region reaches the surface, the depletion region of the vertical junction will extend along the surface over a much longer distance than can be predicted from a simple one-dimensional calculation. This behavior implies a strong reduction of the surface electric field. Below a certain thickness, the surface field will not reach the critical value, and the bulk field will arrive at E_{crit} first. Breakdown voltage is then determined by the horizontal junction, and the ideal bulk breakdown (Fig. 5.2b) can be realized. If the epitaxial layer is too thin, this can be considered



a. Thick epitaxial layer



b. Thin epitaxial layer

Fig. 5.2. ELECTRIC-FIELD DISTRIBUTION.

to be a punchthrough diode; the vertical P^+N^- can be neglected, and the breakdown voltage is thereby determined by the $N^+N^-P^-$ diode.

Because the interaction of the vertical- and horizontal-junction depletion layers is highly two dimensional, a two-dimensional numerical analysis is required to calculate the breakdown voltages. For a given substrate ($N_{A(sub)} = 1.7 \times 10^{14}$ cm^{-3}) and epitaxial ($N_{D(epi)} = 6 \times 10^{14}$ cm^{-3}) doping concentration, the calculated breakdown voltage is plotted in Fig. 5.3 as a function of epitaxial-layer thickness (assuming that the lateral distance between the N^+ and P^+ diffusions is very much greater than the layer thickness). There is an optimal epitaxial thickness at which breakdown occurs at the $N^+N^-P^-$ bulk junction and where breakdown voltage is maximized (region ②). On each side of this thickness, the breakdown voltage drops as the result of field crowding near

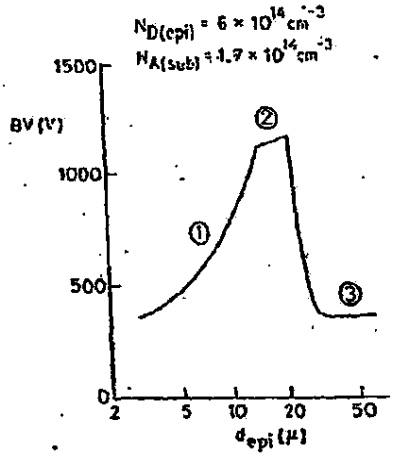


Fig. 5.3. BREAKDOWN VOLTAGE AS A FUNCTION OF EPITAXIAL THICKNESS. Epitaxial and substrate doping concentrations are constant [5.5].

either the P^+N^- (region ③) or $N^+N^-P^-$ (region ①) junction. The optimal thickness is established when $N_{D(epi)} \cdot d_{epi} = 1 \times 10^{12}\ cm^{-2}$. Figure 5.4 illustrates how breakdown voltage depends on epitaxial doping concentration after $N_{A(sub)}$ and d_{epi} are known [5.6]. As can be seen in Fig. 5.3, the maximum breakdown voltage appears at the point where $N_{D(epi)} \cdot d_{epi} = 1 \cdot 10^{12}\ cm^{-2}$.

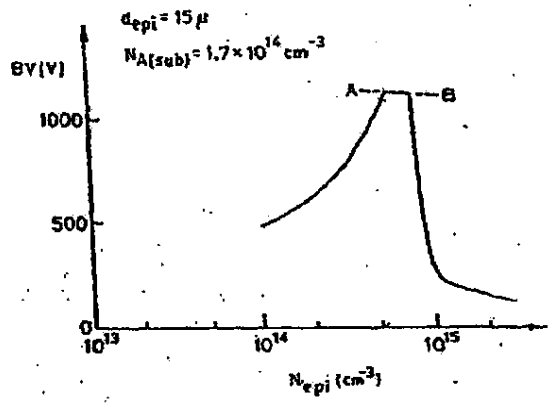


Fig. 5.4. BREAKDOWN VOLTAGE AS A FUNCTION OF EPITAXIAL DOPING CONCENTRATION. The dotted line between A and B represents the theoretical breakdown voltage of the $N^+N^-P^-$ horizontal junction [5.6].

5. Similarity between RESURF and Ion-Implanted Offset-Gate MOSFETs

Erb and Dill [5.7] first proposed the ion-implanted offset-gate (or "extended drain") MOSFET in Fig. 5.5 wherein the completely depleted offset region greatly reduces the drain field. The advantage of this structure is that breakdown voltage can be controlled by adjusting the ion dose. This configuration has been modified for the silicon-on-sapphire (SOS) transistor in Fig. 5.6 [5.2] and for the LMOS transistor in Fig. 5.7 [5.3].

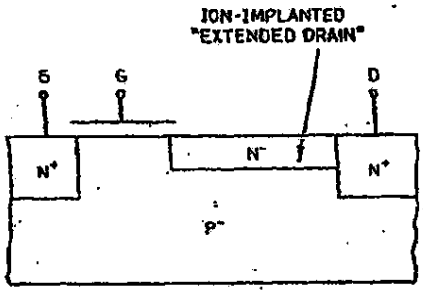


Fig. 5.5. CROSS SECTION OF AN ION-IMPLANTED OFFSET-GATE HIGH-VOLTAGE MOSFET [5.7].

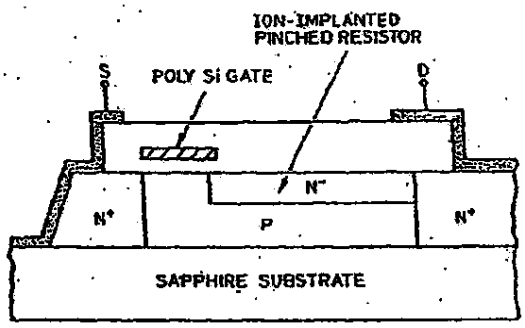


Fig. 5.6. CROSS SECTION OF THE OFFSET-GATE SOS/MOS TRANSISTOR [5.2].

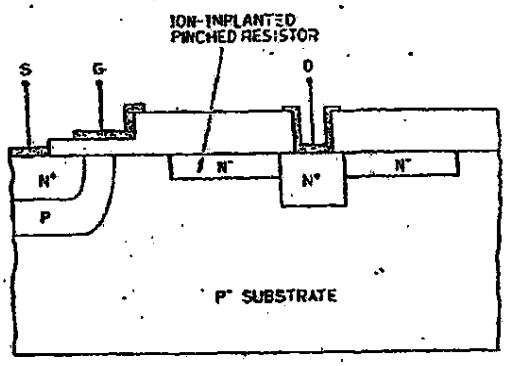


Fig. 5.7. CROSS SECTION OF THE HIGH-VOLTAGE DMOS TRANSISTOR [5.3].

In both the offset-gate and RESURF MOSFETs, a JFET (pinched resistor) between the active low-voltage region and the high-voltage contact region is introduced to reduce the surface field. The equivalent circuit in Fig. 5.8 is represented by an MOS transistor in series with a JFET.

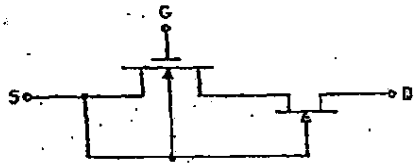


Fig. 5.8. EQUIVALENT CIRCUIT OF THE STRUCTURES IN FIGS. 5.5, 5.6, AND 5.7.

The portion of the offset gate in Fig. 5.5 is redrawn in Fig. 5.9 wherein the ion-implanted N^- region is deeper than the N^+ drain contact. The resemblance between the two structures is apparent. When the N^- region is ion implanted, it becomes an offset gate and, when it is epitaxially grown, it becomes RESURF. There is also an optimal ion-implanted dose to maximize the breakdown voltage, and Fig. 5.10 plots this voltage as a function of dosage [5.3]. When the ion dose is high, avalanche breakdown occurs at the terminal of the N^- region to the source (Ⓐ in Fig. 5.9) and this region is not depleted; when the dose is low,

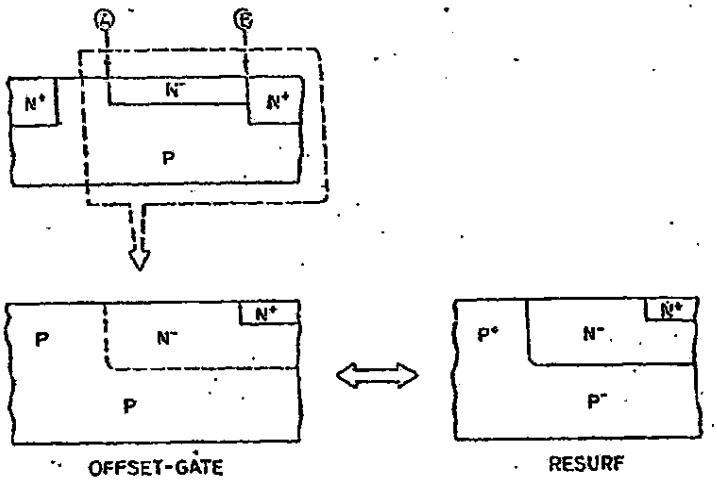


Fig. 5.9. SIMILARITY BETWEEN OFFSET-GATE AND RESURF MOSFETs.

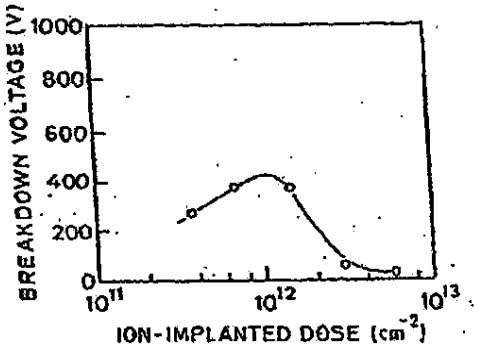


Fig. 5.10. BREAKDOWN VOLTAGE AS A FUNCTION OF ION-IMPLANTED DOSE. Substrate doping is 1.5×10^{14} cm^{-3} [5.3].

the N^- region is completely depleted and breakdown occurs at the terminal of the N^+ drain region (Ⓑ in Fig. 5.9). The optimal ion-implanted dose is experimentally determined to be nearly equal to 1.1×10^{12} cm^{-2}.

3. Derivation of $N_{D(epi)} \cdot d_{epi} \approx 1 \times 10^{12}$ cm^{-2} at Ideal Bulk Breakdown

As noted above, the ion-implanted offset-gate region or the thin epitaxial layer can be regarded as a pinched resistor (JFET). To

prevent breakdown at the vertical P^+N^- junction in the RESURF or at the end of the N^- implanted region near the source in the offset gate, the N^- region should be completely depleted before the P^+N^- junction (in RESURF) or P^-N junction (in the offset gate) reaches E_{crit}. In the RESURF structure, for example, the depletion-layer width on the side of the epitaxial layer is

$$X_d = \left[\frac{2\epsilon_{si}N_{A(sub)}V_a}{q(N_{A(sub)} + N_{D(epi)})N_{D(epi)}}\right]^{1/2} \tag{5.1}$$

where V_a is the applied potential and the built-in potential is neglected. At $V_a = BV$, the electric field at or near the P^+N^- junction, as determined in Eq. (2.7), is

$$BV = \frac{\epsilon_{si}E_{crit}^2}{2qN_{D(epi)}} \tag{5.2}$$

which, when substituted into Eq. (5.1), should yield the depletion-layer width at the P^+N^- junction breakdown when the epitaxial layer becomes too thick. To avoid this problem, d_{epi} should be less than the X_d value; that is,

$$d_{epi} \le \left[\frac{2\epsilon_{si}N_{A(sub)}}{q(N_{A(sub)} + N_{D(epi)})N_{D(epi)}} \frac{\epsilon_{si}E_{crit}^2}{2qN_{D(epi)}}\right]^{1/2} \tag{5.3}$$

By rearranging, the following condition is obtained:

$$N_{D(epi)} \cdot d_{epi} \le \frac{\epsilon_{si}}{q}\left[\frac{N_{A(sub)}}{N_{A(sub)} + N_{D(epi)}}\right]^{1/2} E_{crit} \tag{5.4}$$

Based on the doping concentrations in Fig. 5.3,

$$N_{A(sub)} = 1.7 \times 10^{14}\ cm^{-3}$$

$$N_{D(epi)} = 6 \times 10^{14}\ cm^{-3}$$

$$E_{crit} = 2.2 \times 10^{5}\ V/cm$$

Eq. (5.4) results in

$$N_{D(epi)} \cdot d_{epi} < 6.75 \times 10^{11}\ cm^{-2}$$

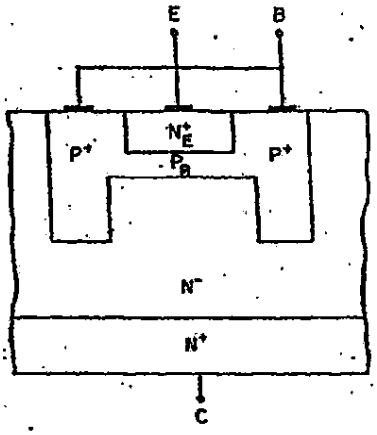
The reason for the discrepancy between this value and $1 \times 10^{12}\ cm^{-2}$ is that a one-dimensional approximation has been used in the derivation of Eq. (5.4), and a two-dimensional numerical calculation is required to obtain the optimal condition.

Another observation in the utilization of a JFET element to achieve high breakdown voltage is the gate-associated transistor (GAT) [5.8] whose schematic and equivalent circuit are shown in Fig. 5.11. The JFET is merged into the base of a standard bipolar transistor. The simultaneous improvements in collector-emitter breakdown voltage and common-emitter current gain are the result of gate shielding that prevents the depletion layer from extending into the base region.

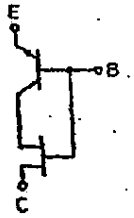
B. Application of RESURF to the LDMOS--Breakdown-Voltage Improvement

1. One-Dimensional Calculation

The LDMOS transistor is important in power-switching IC applications because its planar configuration (all three electrodes on the topside surface) is attractive when combining high-voltage transistors and low-voltage circuitry on the same chip. The geometry of its active region is illustrated in Fig. 5.12. A LDMOS with a 5 Ω-cm, 25 μ epitaxial layer on a 15 to 30 Ω-cm P^- substrate will break down at approximately 250 V [5.9] as a result of channel junction curvature and field crowding near the source-contact metallization edges. A LDMOS with a thinner epitaxial layer (5 Ω-cm, 14 μ) on a 7 Ω-cm p-type substrate has been designed [5.10] to achieve a 400 V BV_{DSS} breakdown voltage. This improvement is the result of the combined field-shaping effects of the channel and substrate junction acting together to deplete the epitaxial drift region.



a. Schematic cross section



b. Equivalent circuit

Fig. 5.11. GATE-ASSOCIATED TRANSISTOR [5.9].

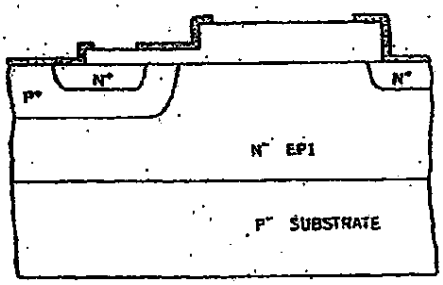


Fig. 5.12. GEOMETRY OF THE LOW-β TRANSISTOR.

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It should be noted that this improvement is only possible when the source and P^- substrate are at the same potential; otherwise, source-to-substrate punchthrough can occur in the thin epitaxy.

Two factors affecting the breakdown of the LDMOS are epitaxial thickness and the separation between the drain and gate-contact metals. This section considers two extreme conditions--very thick and very thin epitaxial layers.

a. Very Thick Epitaxial Layer

LDMOS breakdown is caused primarily by channel junction curvature and, as a result, the P^- substrate can be neglected. A first-order approximation of this breakdown voltage is based on a cylindrical junction formulation [5.11],

$$BV = \left\{ \frac{1}{2} \left[\left(\frac{r_j}{W'} \right)^2 + 2 \left(\frac{r_j}{W'} \right)^{6/7} \right] \ln \left[1 + 2 \left(\frac{W'}{r_j} \right)^{8/7} \right] - \left(\frac{r_j}{W'} \right)^{6/7} \right\} BV_{pp} \qquad (5.5)$$

where

r_j = channel junction depth (μ)

BV_{pp} = plane breakdown voltage [Eq. (2.2)]

$W' = 2.57 \times 10^{-2} \, BV_{pp}^{7/6}$ (μ)

With an epitaxial doping of 1×10^{15} cm^{-3} and $r_j = 5$ μ, Eq. (5.5) yields 147 V which agrees well with the measured data; however, when the source metal field plate overlaps the junction, this voltage increases to ≈250 V.

b. Very Thin Epitaxial Layer

The N^- epitaxial drift region becomes depleted long before the channel junction reaches the critical field; here, the effect from the channel junction can be neglected, breakdown will occur between the drain and substrate, and the derivation becomes that for an $N^+S^-P^-$ punch-through diode. In Chapter II, the one-sided abrupt P^+N^- diode-breakdown

calculation (one-dimensional) was considered. For abrupt P^-N^- junctions having doping levels of N_A and N_D, breakdown voltage can also be obtained from Eq. (2.2) by using an effective doping concentration N_{eff} [5.12] such that

$$\frac{1}{N_{eff}} = \frac{1}{N_A} + \frac{1}{N_D} \tag{5.6}$$

Substituting this N_{eff} into Eq. (2.2), the breakdown voltage in a P^-N^- junction becomes

$$BV \cong 2.932 \times 10^{12} N_{eff}^{-0.666} \tag{5.7}$$

from which the critical field can be derived [based on Eq. (2.7)] as

$$E_{crit} = \left(\frac{2 \times 2.932 \times 10^{12} q N_{eff}^{0.334}}{\epsilon_{si}} \right)^{1/2} \tag{5.8}$$

After determining E_{crit}, the following calculation of the breakdown voltage of an $N^+N^-P^-$ punchthrough diode BV_{PT} becomes straightforward. In Fig. 5.13, a one-dimensional Poisson equation was solved.

For $x < 0$,

$$\frac{dE}{dx} = \frac{qN_{A(sub)}}{\epsilon_{si}} \tag{5.9}$$

and, after integration,

$$E_{max} = \frac{qN_{A(sub)}}{\epsilon_{si}} X_p \tag{5.10}$$

For $x \geq 0$,

$$\frac{dE}{dx} = -\frac{qN_{D(epi)}}{\epsilon_{si}} \tag{5.11}$$

and, after integration,

$$E_1 \leq E_{crit} - \frac{qN_{D(epi)}}{\epsilon_{si}} dx \tag{5.12}$$

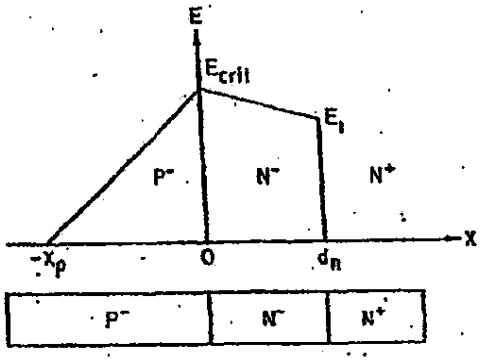


Fig. 5.13. ELECTRIC FIELD OF AN $N^+N^-P^-$ DIODE AT AVALANCHE BREAKDOWN.

Punchthrough breakdown voltage then becomes

$$BV_{PT} = \frac{1}{2} X_p E_{crit} + \frac{1}{2} (E_{crit} + E_1) \, dn \qquad (5.13)$$

which, after substituting Eqs. (5.10) and (5.12) into it, yields

$$BV_{PT} = \frac{E_{crit}^2 \varepsilon_{si}}{2qN_{A(sub)} + E_{crit} \, dn} - \frac{qN_{D(epi)} dn^2}{2\varepsilon_{si}} \qquad (5.14)$$

where dn is the spacing between the drain and substrate.

These calculations have been confined to plane junctions. Taking the N^+ drain-diffusion curvature into account, BV_{PT} can be modified by a cylindrical-junction approximation.

First, punchthrough voltage V_p [5.13] is

$$V_p = \frac{qN_{D(epi)} dn^2}{2\varepsilon_{si}} \qquad (5.15)$$

The breakdown voltage of the punchthrough diode with a cylindrical N^+ junction BV_{cy} is then related to V_{PT} and V_p through two factors,

$$BV_{cy} = F_{1cy} BV_{pT} + F_{2cy} W_T \qquad (5.16)$$

where

$$F_{1cy} = (6)^{1/7} \left(\frac{r_{jn}}{dn}\right)^{6/7} \ln\left(1 + \frac{W_I'}{r_{jn}}\right)$$

$$F_{2cy} = \left(\frac{r_{jn}}{dn}\right)^{2} \left(1 + \frac{W_I'}{r_{jn}}\right)^{2} \ln\left(1 + \frac{W_I'}{r_{jn}}\right) - 1$$

Here, W_I' is the equivalent depletion-layer width at the curved N^+ diffusion and is related to dn by

$$\left(\frac{dn}{r_{jn}}\right)^2 = \left(1 + \frac{W_I'}{r_{jn}}\right)^2 \ln\left(1 + \frac{W_I'}{r_{jn}}\right) - \frac{1}{2}\left[\left(1 + \frac{W_I'}{r_{jn}}\right)^2 - 1\right] \qquad (5.17)$$

where r_{jn} is the N^+ diffusion depth. For $r_{jn} = 2$ [illegible], $dn = 3$ μ, and $N_{D(epi)} = N_{A(sub)} = 1 \times 10^{15}$ cm^{-3}, the calculated BV_{cy} is 224 V.

2. Two-Dimensional Calculation

In the intermediate range of epitaxial-layer thickness, a two-dimensional numerical simulation is required to calculate the breakdown voltage. The computer program used in this study was CANDE (Computer Analysis of Nonplanar DEvices) [5.14] that solves Poisson's equation with the appropriate boundary conditions via a two-dimensional depletion-region approximation within the semiconductor. This computation of avalanche breakdown voltages by CANDE begins by first solving Poisson's equation with a specified bias. Following completion of the field calculations, an avalanche ionization integral is formulated by first determining the path of multiplication and then calculating the integrals.

To determine the path, a single electric-field line is identified by the location of a starting point, which is generally the point of the highest electric field in the device because the path of maximum

multiplication normally passes through it. The electric-field line is then followed in both directions along the path of the potential gradient until the field becomes negligible. If the path reaches the interface between the semiconductor and insulator, it can be modified so that it will remain in the semiconductor and the field component is taken in that direction.

After the fields and spacings along the multiplication path are determined, the ionization integral is then calculated. The avalanche breakdown voltage at which the integral is unity is obtained iteratively by changing the applied bias.

The device dimensions of the LDMOS used in the simulation are shown in Fig. 5.14, and its simulated breakdown voltage is plotted in Fig. 5.15 as a function of epitaxial-layer thickness at two substrate dopings; the calculated results obtained for both thick [Eq. (5.5)] and thin [Eq. (5.10)] layers are also plotted for comparison. For thin layers, the agreement between simulation and calculation is within 5 percent; for thick layers, the simulation more closely resembles the experimental data reported in Ref. 5.9 because of the use of field plates. The calculated voltage is lower than the simulated value because no field plate overlapped the junction.

As described in Section A (Fig. 5.3), there is an optimal epitaxial-layer thickness at which the breakdown voltage is maximized.

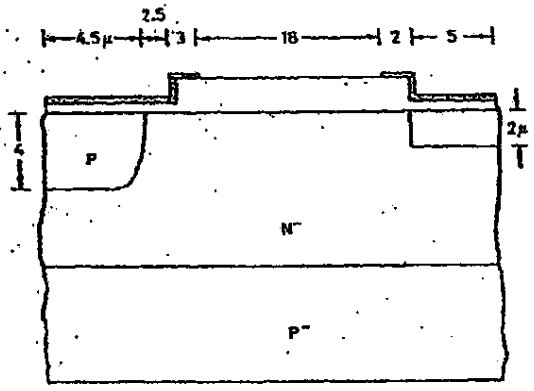


Fig. 5.14. DEVICE DIMENSIONS IN THE CANDE SIMULATION.

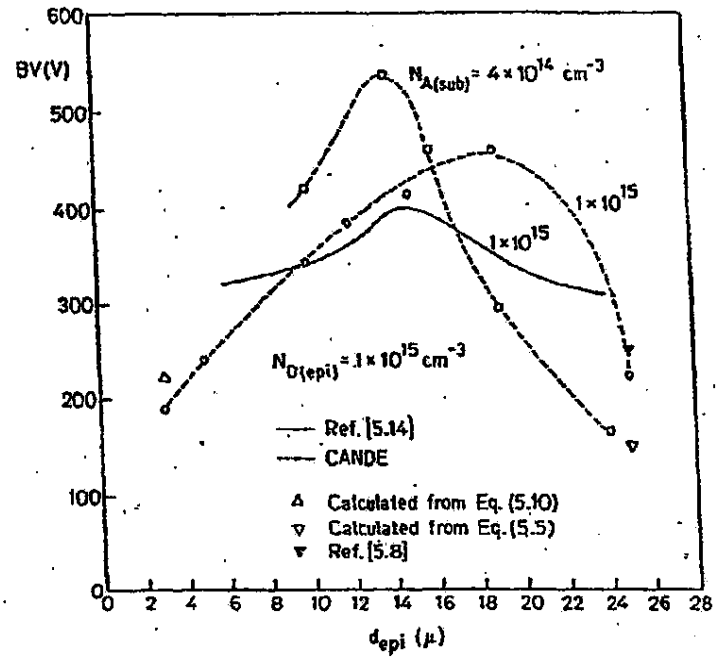


Fig. 5.15. BREAKDOWN VOLTAGE VS EPITAXIAL-LAYER THICKNESS OF THE LDMOS IN FIG. 5.14.

Because the calculation of electric field on the semiconductor side near the interface incorrectly used the average values of ε_{si} and ε_{ox} in the original CANDE program, this error produced a higher electric field along the path of multiplication near the interface. As a result, the simulated voltages obtained from CANDE are higher than those in Ref. 5.14 when surface breakdown occurs ($d_{epi} > 16$ μ). Apart from the absolute values of BV, however, it becomes apparent in Fig. 5.15 that the peak breakdown voltage increases and the epitaxial thickness at which breakdown is maximized decreases when P^- substrate doping becomes lighter. This can be understood from Eq. (5.4). As $N_{A(sub)}$ doping is reduced, both $[N_{A(sub)}/(N_{A(sub)}+N_{D(epi)})]^{1/2}$ and E_{crit} become smaller which lowers the $N_{D(epi)} \cdot d_{epi}$ product. Because $N_{D(epi)}$ is constant, this means that the optimal d_{epi} will be reduced.

The effect of separation d between the gate and drain metallizations is plotted in Fig. 5.16 [5.15]. As d is increased, the breakdown voltage rises (upper curve) and, if d is further increased, BV will approach the limit determined by the substrate doping level. From Eq. (5.14) where $N_{A(sub)} = N_{D(epi)} = 1 \times 10^{15}$ cm^{-3} and dn = 15 μ, this limit is ≈470 V.

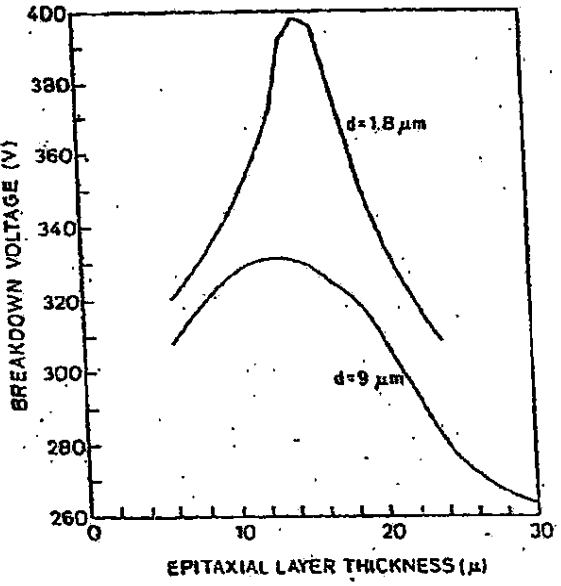


Fig. 5.16. BREAKDOWN VOLTAGE VS EPITAXIAL-LAYER THICKNESS FOR TWO VALUES OF SPACING BETWEEN THE GATE AND DRAIN METALLIZATIONS [5.15].

To reduce device on-resistance, d must be as small as possible and epitaxial doping and thickness must be large. Because the impurity density of the substrate is low in devices having high breakdown voltages, however, the total impurity dose $[\int N_{D(epi)}\, dx]$ in the epitaxial layer must be light enough to maintain a low surface field near the gate edge. In addition, d must be long enough to achieve high voltages. These structural parameters must be optimized using a two-dimensional numerical analysis, such as CANDE.

C. Variations of the RESURF LDMOS—On-Resistance Reduction

The epitaxial-layer requirement of $N_{D(epi)} \cdot d_{epi} \cong 1 \times 10^{12}\ cm^{-3}$ sets an upper bound on the current-handling capability and a lower bound on device on-resistance. To reduce on-resistance, the $N_{D(epi)} \cdot d_{epi}$ product must be increased and the epitaxial resistivity in the major portion of the current path must be minimized without lowering the breakdown voltage. The following variations of the RESURF LDMOS are based on these two considerations.

1. Field Shaping via a Buried Layer [5.15]

As indicated in Eq. (5.4), the $N_{D(epi)} \cdot d_{epi}$ product can be made larger if the level of substrate doping $N_{A(sub)}$ is raised. To avoid lowering the breakdown voltage, however, $N_{A(sub)}$ is not increased indiscriminately; only the portion under the channel is increased so that the epitaxial drift region above it can be depleted to reduce the channel-junction surface field. Because the breakdown voltage is determined by the drain-substrate junction, the substrate under the drain region will have a lighter doping concentration. The LDMOS in Fig. 5.17 is an example of this field-shaping buried-layer method and is analogous to the multiple-implant offset-gate structure in Fig. 5.18 [5.16]. In both devices, on-resistance has been reduced without lowering the breakdown voltage.

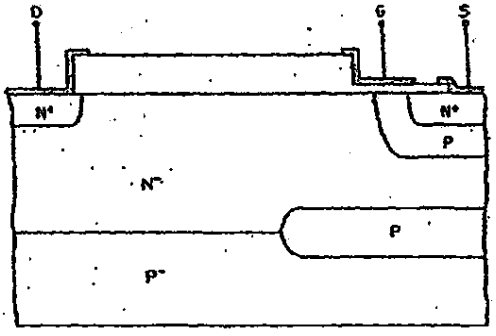


Fig. 5.17. LDMOS WITH A BORON-IMPLANTED BURIED LAYER UNDER THE CHANNEL REGION.

The factors affecting the breakdown of this boron-implanted LDMOS are epitaxial-layer thickness and the separation between the buried layer and drain. The CANDE program has been used to investigate these two parameters.

a. Effect of Epitaxial-Layer Thickness

Three epitaxial thicknesses (9, 6, and 5 μ) were analyzed. The electric field lines and equipotential contours in Fig. 5.19a and b are those of a 9 μ device. Lines of the constant electric field are plotted in Fig. 5.19c, and the location of maximum field is indicated by the 2.8×10^5 V/cm curve. The epitaxial and substrate dopings were 3×10^{15} and 4×10^{14} cm^{-3}, respectively, and the boron-implanted buried layer was 4.5 μ thick with a 4×10^{15} cm^{-3} doping concentration. It should be noted that $N_{A(sub)}$ and $N_{D(epi)}$ varied substantially from the concentrations used in the LDMOS in Fig. 5.15. The calculated breakdown voltage was ≈310 V, and the breakdown occurred at the silicon surface near the gate metal edges. Because the epitaxial layer was too thick, the highest electric-field points were close to the channel junction (Fig. 5.19c).

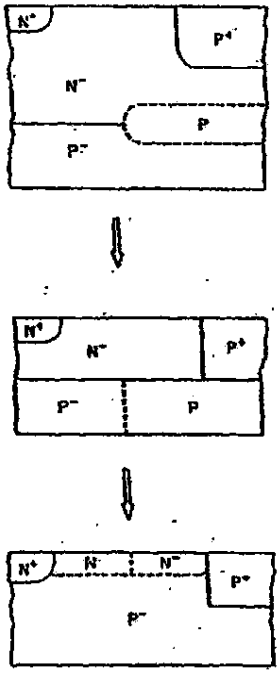
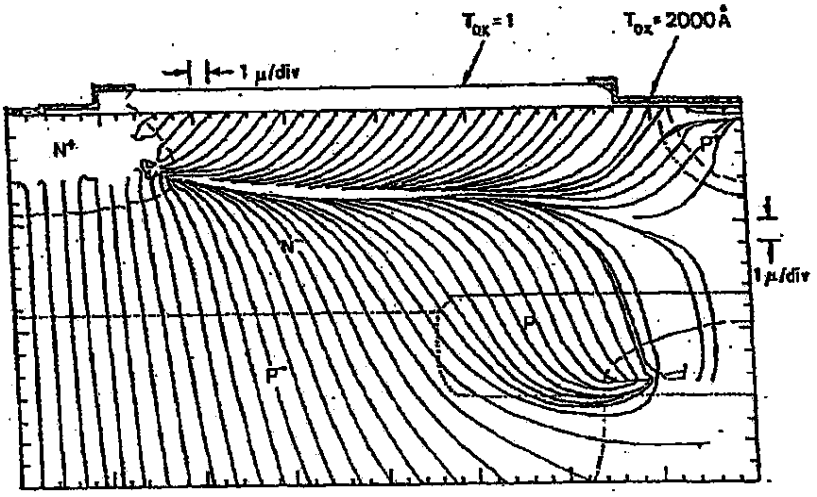
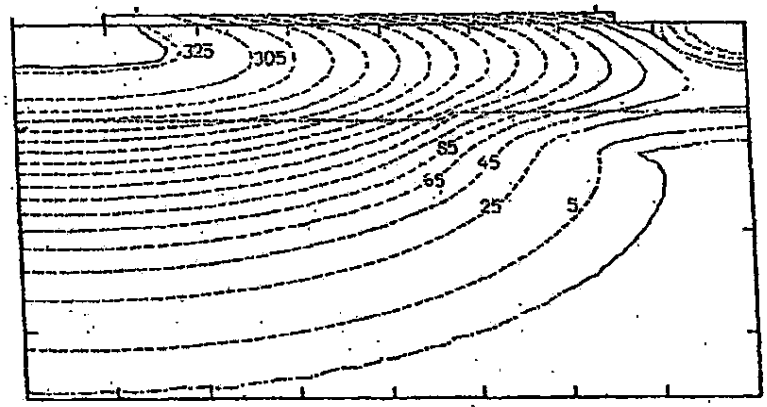


Fig. 5.18. ANALOGY BETWEEN A BURIED-LAYER RESURF AND A MULTIPLE-IMPLANT OFFSET-GATE STRUCTURE.

As the epitaxial thickness was reduced to 6 μ, the highest electric-field points shifted to the N^-P^- junction under the drain (Fig. 5.20) and the breakdown voltage increased to 400 V. As the thickness was further reduced to 5 μ, the field under the drain intensified and the breakdown voltage dropped back to 385 V (Fig. 5.21).

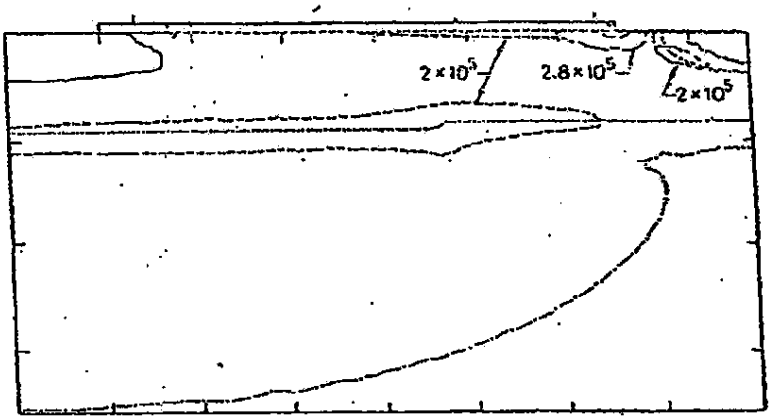


a. Electric-field line distribution



b. Equipotential contour

Fig. 5.19. RESULTS OF A COMPUTER SIMULATION OF THE LDMOS WITH A BORON-IMPLANTED BURIED LAYER UNDER THE CHANNEL REGION. Epitaxial thickness = 9 μ and breakdown voltage = 310 V.



c. Electric-field contour

Fig. 5.13. CONTINUED.

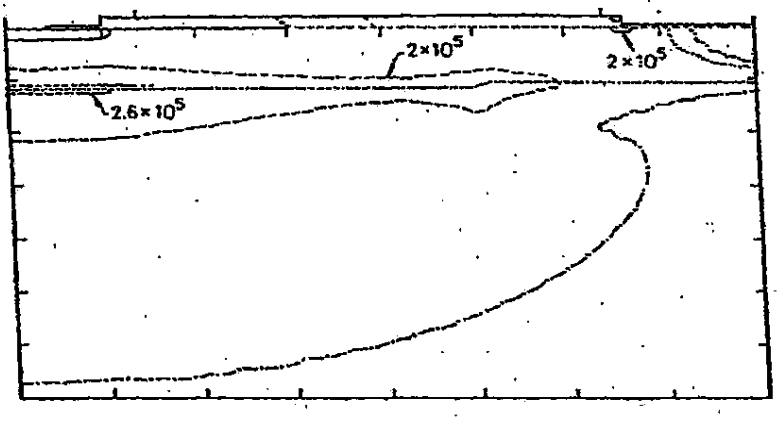


Fig. 5.20.. ELECTRIC-FIELD CONTOUR OF THE LDMOS IN FIG. 5.17 WITH AN EPITAXIAL THICKNESS OF 6 μ. Breakdown voltage = 400 V, and the distance between the drain and buried layer = 20 μ.

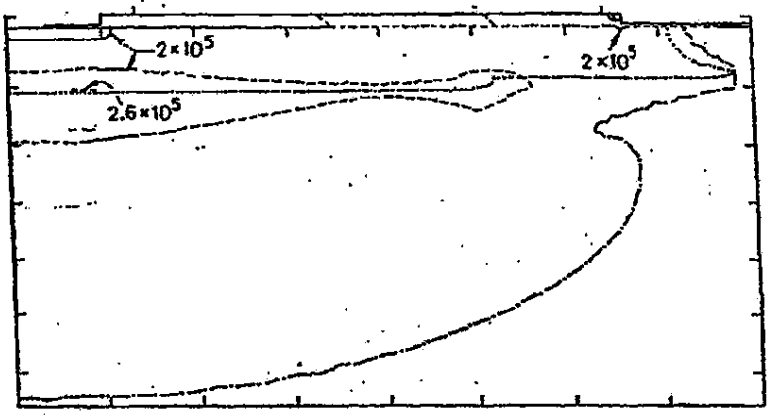


Fig. 5.21. ELECTRIC-FIELD CONTOUR OF THE LDMOS IN FIG. 5.17 WITH AN EPITAXIAL THICKNESS OF 5 μ. Breakdown voltage = 385 V.

b. Effect of the Distance between Buried Layer and Drain

In the LDMOS with a 6 μ epitaxial layer (Fig. 5.20) where the breakdown voltage was maximized to 400 V, the separation between the buried layer and drain was 20 μ. If this distance is reduced to 12 μ, the peak electric-field points will no longer appear at the P^-N^- junction under the drain (Fig. 5.20) but at the buried-layer junction, as shown in Fig. 5.22, and the breakdown voltage will drop to 325 V. This behavior is similar to the RESURF LDMOS where the distance between the gate and drain metallizations is important; the only difference is that one is bulk breakdown (buried-layer LDMOS) and the other is surface breakdown (RESURF LDMOS) as the separation becomes too small.

2. Two-Region Profile of the Epitaxial Layer

The RESURF requirement that $N_{D(epi)} \cdot d_{epi} \approx 10^{12}$ cm^{-2} actually should be $\int N_{D(epi)}\, dx \approx 10^{12}$ cm^{-2}. It is the total impurity dose in the epitaxial layer that accounts for the depletion of this layer. This observation opens the way to many possibilities for the epitaxial impurity profile for specific device applications. Vaes and Appels [5.17] used two epitaxial doping regions for JFET applications, and this concept can also be applied in the LDMOS. Figure 5.23 is a cross section of the

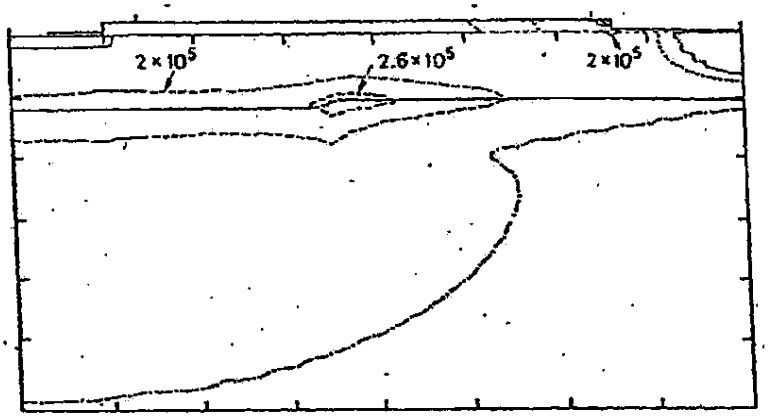


Fig. 5.22. ELECTRIC-FIELD CONTOUR OF THE LDMOS IN FIG. 5.17 WITH A 6 μ EPITAXIAL THICKNESS AND A 12 μ DISTANCE BETWEEN THE DRAIN AND BURIED LAYER. Note the variation in the location of the highest field from that in Fig. 5.20.

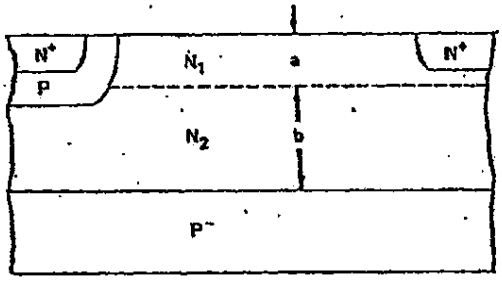


Fig. 5.23. CROSS SECTION OF A LDMOS WITH A TWO-REGION EPITAXIAL PROFILE.

proposed structure wherein N_1 has a higher doping concentration than does N_2; however, the total doping integral $N_1a + N_2b$ is still $\approx 1 \times 10^{12}$ cm^{-2}. As discussed in the on-resistance modeling of the LDMOS in Chapter II, most current flows near the silicon surface because the carriers are injected and then collected by the regions near the surface; in addition, the carrier will travel the shortest distance. As a result, a higher doping concentration in the upper portion of the epitaxial layer will improve the current-carrying capability. Optimization of this structure, however, is nontrivial. It must satisfy such requirements as

- $N_1 a + N_2 b \approx 10^{12}$ cm^{-2}
- meet a specific breakdown voltage which is a function of N_2, b, and $N_{A(sub)}$
- minimize on-resistance which is a function of N_1, a, N_2, b, and the distance between the channel and drain

The solution of this problem would require numerical techniques and a trial-and-error approach to optimization.

D. Summary

This chapter has studied a new structure with a thin epitaxial layer and has considered its application in LDMOS transistors. The basic principle is the interaction of the surface and substrate junctions (depletion-charge sharing) to minimize the surface field. The similarity between the RESURF and ion-implanted offset-gate LDMOS devices has been analyzed, and the observed differences between them are very minor. First-order analytical approaches have been followed to calculate two extreme conditions--thick and thin epitaxial layers. Two-dimensional computer simulation becomes a necessity in optimizing the device parameters to increase the breakdown voltage and to lower on-resistance. Two variations of the basic RESURF LDMOS were investigated in an attempt to reduce device on-resistance.

Chapter VI

CONCLUSIONS AND RECOMMENDATIONS

A. Conclusions

The voltage, current, and power ratings of power MOS transistors developed from recent technological advances are comparable to bipolar transistors but have all of the performance advantages of MOSFETs. Device design, fabrication, and static theory have been described.

The major contributions of this research are as follows.

- Quantitative models, expressed in simple analytical equations and suitable for device design, have been developed to determine the on-resistance of the LDMOS, VDMOS, and VMOS. They were obtained directly from the geometry and doping profiles and were found to be useful in quantitatively comparing the devices.

- The usefulness of the model in optimizing a particular structure was illustrated by a VDMOS with hexagonal layout geometries for a specific application (breakdown voltage = 450 V).

- Vertical DMOS transistors with narrow p-well spacings exhibit two pronounced saturation regions, and this behavior has been described successfully in terms of depletion-region pinchoff of the lightly doped epitaxial region between the channel junctions. A first-order drain voltage-current solution has been obtained to demonstrate the dependence of this phenomenon on the physical structure. The degradation of this effect on device transconductance can be more severe than the thermal effect in high-current operations.

- The limitations of punchthrough voltage and parasitic bipolar latchback have been analyzed for vertical power MOSFETs. The results indicate that the switching requirement dV/dt during turn-off places a more severe constraint on channel thickness and doping concentration under most layout conditions. The punchthrough limit is significant only when the channel contacts are adjacent to the edges of the gates.

- A modified Johnson's limit (a figure of merit between maximum voltage and frequency) and its associated parametric dependence have been analyzed. The differences between power MOS and bipolar transistors were identified in terms of carrier injection and transport mechanisms.

- Extensive experimental measurements of electron inversion and accumulation-layer mobility were completed. Empirical equations were developed to facilitate the calculation of electron mobility under a wide variety of substrate, process, and electrical conditions at low V_{DS}. From the observed effects of the processing parameters on mobility rolloff under high vertical fields, the optimal processing conditions for maximizing mobility could be determined. This work was motivated by a lack of adequate mobility data in the literature for power MOS device modeling.

- A recently developed RESURF LDMOS has been analyzed to understand its high breakdown voltages and performance trade-offs between on-resistance and breakdown voltage. A one-dimensional analytical method was used when possible, and a two-dimensional numerical simulation was employed when the interaction between the surface and substrate junctions became important.

B. Recommendations

The analysis presented in this work was confined to dc device characteristics. An ac analysis, especially of high-frequency performance, should prove to be an important study of power MOS devices.

A more accurate model is required for the JFET in the I-V modeling of a VDMOS with narrow p-well spacings. This would include bulk mobility as a function of electric field, velocity saturation, and more sophisticated junction profiles instead of rectangular geometries. Two-dimensional numerical techniques may be necessary.

In the area of electron mobility, a natural extension of this work would be the study of weak-inversion mobility which is a basic parameter in modeling subthreshold I-V characteristics. A limited amount of data has been obtained; however, a more precise data analysis and its correlation with theoretical work are needed to further understand the impact of processing conditions on the behavior of weak-inversion mobility.

Appendix A

EFFECTS OF DRAIN AND SOURCE RESISTANCES ON THE TRANSCONDUCTANCE OF MOSFETs

Transconductance in the linear region is often confused with transconductance in the saturation region when both drain resistance R_D and source resistance R_S are present [A.1,A.2]. This appendix attempts to clarify some of the differences.

Referring to Fig. A.1, the drain current in the linear region in simple form is

$$I_D = \beta(V_{GS} - V_T)\, V_{DS} \qquad (A.1)$$

where

$$\beta = \frac{W}{L}\mu C_o$$

Expressing I_D in terms of R_S and R_D,

$$I_D = \beta(V_G - I_D R_S - V_T)\left[V_D' - I_D(R_D + R_S)\right] \qquad (A.2)$$

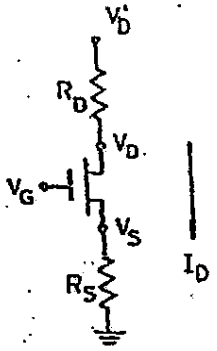


Fig. A.1. EQUIVALENT CIRCUIT USED IN THE CALCULATION OF TRANSCONDUCTANCE.

Transconductance when R_S and R_D are present is defined as

$$g_m' = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D'=\text{constant}} \tag{A.3}$$

Differentiation yields

$$g_m' = \beta\left[V_D' - I_D(R_D + R_S)\right](1 - R_S g_m') + \beta(V_G - I_D R_S - V_T)\left[-(R_D + R_S)\, g_m'\right] \tag{A.4}$$

The intrinsic transconductance, however, is

$$g_m = \beta V_{DS} \tag{A.5}$$

and the intrinsic conductance is

$$g_d = \beta(V_{GS} - V_T) \tag{A.6}$$

which, when substituted into Eq. (A.4) and rearranging, becomes

$$g_m' = \frac{g_m}{1 + g_m R_S + g_d(R_S + R_D)} \tag{A.7}$$

This is the transconductance in the linear region.

In simple form, the saturation drain current is

$$I_D = \frac{\beta(V_{GS} - V_T)^2}{2} \tag{A.8}$$

where

$$V_{GS} = V_G - I_D R_S \tag{A.9}$$

Transconductance in the saturation region is defined as

$$g_m^* = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D'=\text{constant}} \qquad \text{(A.10)}$$

Substituting Eq. (A.9) into (A.8) and differentiating yields

$$g_m^* = \beta(V_G - V_T - I_D R_S)(1 - R_S g_m^*) \qquad \text{(A.11)}$$

or

$$g_m^* = \frac{\beta(V_G - V_T - I_D R_S)}{1 + R_S\beta(V_G - V_T) - \beta R_S I_D R_S} \qquad \text{(A.12)}$$

From Eqs. (A.8) and (A.9),

$$I_D R_S = \frac{\beta R_S}{2}(V_G - V_T - I_D R_S)^2 \qquad \text{(A.13)}$$

which, when solving for $I_D R_S$, can be expressed as

$$I_D R_S = (V_G - V_T) + \frac{1}{\beta R_S} + \left[\left(\frac{1}{\beta R_S}\right)^2 + \frac{2(V_G - V_T)}{\beta R_S}\right]^{1/2} = f(V_G - V_T, \beta R_S) \qquad \text{(A.14)}$$

By substituting this expression into (A.12), the transconductance in the saturation region takes the form of

$$g_m^* = \frac{\beta\left[V_G - V_T - f(V_G - V_T, \beta R_S)\right]}{1 + R_S\beta(V_G - V_T) - \beta R_S f(V_G - V_T, \beta R_S)} \qquad \text{(A.15)}$$

The major difference between linear g_m' and saturation g_m^* becomes apparent after examining Eqs. (A.7) and (A.15).

- Transconductance in the linear region is a function of both R_S and R_D.
- Transconductance in the saturation region depends on R_S only and is independent of R_D.

Appendix B

SOLUTION OF POISSON'S EQUATION FOR A CYLINDRICAL ABRUPT ONE-SIDED JUNCTION

Referring to Fig. B.1, Poisson's equation in the cylindrical coordinates on the N^- side [B.1] is

$$\frac{d^2V}{dr^2} + \frac{1}{r}\frac{dV}{dr} = \frac{-\rho(r)}{\varepsilon_{si}} \tag{B.1}$$

where

$$\rho(r) = qN_D \tag{B.2}$$

Integrating both sides of Eq. (B.1),

$$\int \frac{d}{dr}\left(r\frac{dV}{dr}\right) = \int \frac{-\rho r}{\varepsilon_{si}}\,dr \tag{B.3}$$

yields

$$r\frac{dV}{dr} = \frac{-\rho r^2}{2\varepsilon_{si}} + A \tag{B.4a}$$

$$\frac{dV}{dr} = \frac{-\rho r^2}{2\varepsilon_{si}} + \frac{A}{r} \tag{B.4b}$$

and integrating again obtains

$$V = \frac{-\rho r^2}{4\varepsilon_{si}} + A \ln (r + B) \tag{B.5}$$

where A and B are the integration constants.

The boundary conditions are

$$V = 0 \quad \text{at} \quad r = X_j$$

$$\frac{dV}{dr} = 0 \quad \text{at} \quad r = X_j \tag{B.6}$$

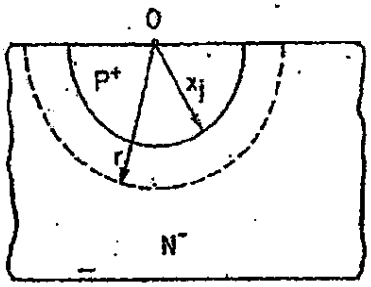


Fig. B.1. CYLINDRICAL ABRUPT JUNCTION.

Applying Eq. (B.6) to Eq. (B.5) and solving for A and B results in

$$A = \frac{\rho x_j^2}{2\epsilon_{si}} \tag{B.7a}$$

$$B = \frac{\rho x_j^2}{4\epsilon_{si}} (1 - 2 \ln x_j) \tag{B.7b}$$

By substituting these definitions into (B.6), the voltage becomes

$$V = \frac{-\rho r^2}{4\epsilon_{si}} + \frac{\rho x_j^2}{2\epsilon_{si}} \ln r + \frac{\rho x_j^2}{4\epsilon_{si}} (1 - 2 \ln x_j) \tag{B.8}$$

and then substituting Eq. (B.2) into (B.8) and rearranging yields

$$V = \frac{qN_D}{4\epsilon_{si}} x_j^2 \left[1 - \left(\frac{r}{x_j}\right)^2 + \ln \left(\frac{r}{x_j}\right)^2\right] \tag{B.9}$$

which is the voltage on the N^- side of a cylindrical P^+N^- junction.

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